REMARKS

Claims 28-33, 38-39, and 52 are pending. Claim 52 has been amended.

This response supplements applicant's amendment dated October 7, 2005. Specifically, applicants respectfully submit a more complete treatment of the outstanding rejection of claim 52 under 35 U.S.C. §112, second paragraph based on indefiniteness. As suggested, applicants point out below exemplary embodiments of the elements or features described in connection with FIG. 4. In addition, claim 52 has been amended. Claim 52 is submitted to particularly point out and distinctly claim the subject matter of applicants' invention.

More specifically, claim 52 has been amended to delete the term "controlled" and now recites a "voltage supply." An exemplary "voltage supply" is shown to include at least element 600 in FIG. 4. In addition, the "electronic charge reservoir" has been amended to be an "electronic charge storage device," an exemplary example of which is capacitor 510. In exemplary example of the current source recited in claim 52 is transistor 770 of FIG. 4. The counter 1000 shown in FIG. 4 represents an exemplary "counter."

Applicants note that the incorrect terms "dock" and "docked" appear at several places throughout the published application 2004/0062100. In each case, the incorrect term was introduced by the Patent Office. Instead of "dock" or "docked," the term should be "clock" or "clocked," respectively. A listing of the misprints is attached to this response.

In view of the above amendment and remarks, in conjunction with applicants response dated October 7, 2005, applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Peter F. McGee
Registration No.: 35,947
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicants

MISPRINTS INTRODUCED TO U.S. PUB. NO. 2004/0062100 A1

Applicants note the following misprints introduced by the Patent Office in U.S. Pub. No. 2004/0062100 A1:

[0026] Thus, even when using digital counting techniques, the discharge time of the capacitor must be counted quite precisely to sense the different resistance values and distinguish logic states. To achieve this precision, either the counting clock must be operated at a high frequency or the capacitor must be discharged relatively slowly. Neither of these options is desirable, since slow capacitor discharge means slow reading of stored memory values, and a high ~~dock~~ clock frequency requires high frequency components. In either case, a counter having a large number of stages is also required.

[0033] The first transistor 710 includes a drain 720 connected to both the selected column line 540 and the inverting input 620 of the first op-amp 600. The first transistor also includes a source 730 operatively connected to a first terminal 740 of a capacitor 510. The capacitor 510 includes a second terminal 750 operatively connected to a ground potential 250. The source 730 of the first transistor 710 is also connected to a drain 760 of a second transistor 770. In this exemplary embodiment, this second transistor 770 is a PMOS transistor. The second transistor 770 includes a source 780 and a gate 790, in addition to the drain 760. The source 780 is operatively connected to a supply voltage 800, which in this exemplary embodiment is 2.5 volts. The gate 790 is operatively connected to an output 900 of a clocked comparator 910. The ~~docked~~ clocked comparator 910, shown as a ~~docked~~ clocked second operational amplifier, includes the output 900, a non-inverting (positive) input 920, an inverting (negative) input 930, and a ~~dock~~ clock input 940 connected to a source of a clock signal 950. The comparator 910 may be implemented as a simple clocked latch, or the comparator 910 may be simply enabled by the ~~dock~~ clock CLK signal.

MISPRINTS INTRODUCED TO U.S. PUB. NO. 2004/0062100 A1 (continued)

[0037] As charge is depleted from capacitor 510 the voltage on the capacitor drops until it falls below the voltage (1 volt) applied to the reference input 920 of the clocked comparator 910. After this threshold is passed, the next positive clock transition applied to the ~~dock~~ clock input 940 causes the output of comparator 910 to go low again turning on the second transistor 770 and causing current to begin flowing through the second transistor 770 to recharge capacitor 510.

[0038] In one embodiment, the capacitor 510 is recharged during one ~~dock~~ clock cycle of ~~dock~~ clock source 950, so the comparator output 900 switches to high and the second transistor 770 is shut off again at the next positive clock transition. Transistor 770 is sized to allow a substantially constant current (e.g., 2.5 μA) to flow to capacitor 510 when transistor 770 is in a conductive state.

[0041] FIG. 5 shows the output signal produced by the clocked comparator when a 100 MHz ~~dock~~ clock signal is applied to the ~~dock~~ clock input 940. At a clock frequency of 100 MHz, clock pulses are spaced at an interval of 10 ns. In the example shown, the output of the clocked comparator is high 1160 for one ~~dock~~ clock pulse (10 ns) and low 1170 for three ~~dock~~ clock pulses (30 ns). This corresponds to the voltage waveform shown in FIG. 6. In FIG. 6, the voltage of the capacitor 510 is shown to begin rising when the output 900 of the clocked comparator goes low (time A), thereby turning on the PMOS transistor 770. The voltage rises for 30 ns, or three clock pulses until time B. At time B, the output of the clocked comparator goes high again, turning off the PMOS transistor. The voltage on the capacitor 510 then begins to drop again while the PMOS device remains off for one clock pulse, or 10 ns (until time C). Accordingly, in the example shown, the duty cycle of the signal output by the ~~docked~~ clocked comparator 910 is 75% (three on-pulses for every off-pulse).

MISPRINTS INTRODUCED TO U.S. PUB. NO. 2004/0062100 A1 (continued)

The following misprint was introduced into claim 19 of U.S. Pat. Pub. 2004/0062100:

19. A resistance measuring circuit comprising: a capacitor having a first terminal; a voltage controlled current source operatively connected to said first terminal, said current source adapted to withdraw current from said capacitor and supply said current to a resistor to be measured, said current source adapted to control said current according to a voltage measured across said resistor; a current pulse generator having an output operatively connected to said first terminal, a clock input adapted to receive a periodic clock signal, and a voltage sensor, said pulse generator adapted to generate a current pulse synchronously with said clock signal whenever said sensor indicates that a voltage at said first terminal is below a threshold voltage, whereby a plurality of current pulses are generated over time; a first counter adapted to count cycles of said periodic ~~dock~~ clock signal to produce a clock count; a second counter adapted to count pulses produced by said pulse generator to produce a pulse count; and a circuit for determining a resistance value of said resistor in response to said pulse count and said clock count.

The following misprint was introduced into claim 24 of U.S. Pat. Pub. 2004/0062100:

24. A memory device as defined in claim 23, wherein said circuit comprises: a first pulse counter having an input receiving a ~~dock~~ clock signal and a second pulse counter having an input receiving an output of said comparator, said circuit determining said resistance by determining the value held in said second counter when said first counter reaches a predetermined value.